## **WEST Search History**

DATE: Monday, September 09, 2002

Set Name	Query	Hit Count			
side by side			result set		
	PT; PLUR=YES; OP=ADJ	_			
L24	L23 and 15 and 122	6	L24		
L23	121 adj4 119	170	L23		
L22	l21 adj4 l20	161	L22		
L21	prefetch or prefetching	3627	L21		
L20	data cache	7021	L20		
L19	instruction cache	4176	L19		
L18	117 and (prefetch or prefetching)	1	L18		
L17	6199142.pn.	1	L17		
L16	115 and 15	6	L16		
L15	L14 and 113	42	L15		
L14	(prefetch or prefetching) adj4 (instruction adj (cache or memory))	226	L14		
L13	(prefetch or prefetching) adj4 (data adj (cache or memory))	220	L13		
L12	18 and 19	10	L12		
L11	18 and 19 and 15	0	L11		
L10	L9 and 18 and 17	0	L10		
L9	data prefetch buffer	84	L9		
L8	instruction prefetch buffer	121	L8		
L7	L5 and (prefetch or prefetching)	93	L7		
L6	15 and 14	1	L6		
L5	Harvard architecture	449	L5		
L4	L3	76	L4		
DB = USPT, PGPB, JPAB, EPAB, DWPI, TDBD; PLUR = YES; OP = ADJ					
L3	(prefetching or prefetch) adj4 11	98	L3		
L2	data adj memory	113340	L2		
L1	(instruction or program or code) adj memory	42021	L1		

END OF SEARCH HISTORY

ST R	Refine Search	WEST SEAKCH	http://westbrs:8002	2/bin/cgi-bin/Pi
	Set Name side by side		Hit Count	Set Name result set
	DB=U	SPT; PLUR=YES; OP=ADJ		
	<u>L25</u>	L24 and 118 and 117	153	<u>L25</u>
	<u>L24</u>	harvard architecture	449	<u>L24</u>
	<u>L23</u>	(memory controller or memory control) same 117 same 118	88	<u>L23</u>
	<u>L22</u>	(memory controller or memory control or controller or control unit or control circuit or control circuitry) same 118 same 117	r 344	<u>L22</u>
	<u>L21</u>	memory controller or memory control or controller or control unit or control circuit or control circuitry	468692	<u>L21</u>
	<u>L20</u>	L19 same 118 same 117	562	<u>L20</u>
	<u>L19</u>	memory controller or memory control or controller or control	1492283	<u>L19</u>
	<u>L18</u>	data adj memory	51781	<u>L18</u>
	<u>L17</u>	(instruction or code) adj memory	10490	<u>L17</u>
	<u>L16</u>	(Rambus or RDRAM) adj interface	50	<u>L16</u>
	<u>L15</u>	L14 and 19	20	<u>L15</u>
	<u>L14</u>	Rambus.asn.	167	<u>L14</u>
	<u>L13</u>	RDRAM.ab.	6	<u>L13</u>
	<u>L12</u>	RDRAM.ti.	1	<u>L12</u>
	<u>L11</u>	L9 same (11 or controller or control) same (instruction or code or command) same data	67	<u>L11</u>
	<u>L10</u>	L9 same (11 or controlle or control) same (instruction or code or command) same data	58	<u>L10</u>
	<u>L9</u>	RDRAM	426	<u>L9</u>
	<u>L8</u>	synchronous dram or SDRAM	3651	<u>L8</u>
	<u>L7</u>	L6	220	<u>L7</u>
	DB=U	SPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
	<u>L6</u>	L5 and 14	319	<u>L6</u>
	<u>L5</u>	11 same (instruction or code or data) same 13 same memory	428	<u>L5</u>
	<u>L4</u>	11 same (instruction or code or data) same 12 same memory	467	<u>L4</u>
	<u>L3</u>	second adj2 bus	12241	<u>L3</u>
	<u>L2</u>	first adj2 bus	11991	<u>L2</u>
	<u>L1</u>	memory adj2 (controller or control)	102166	<u>L1</u>

END OF SEARCH HISTORY